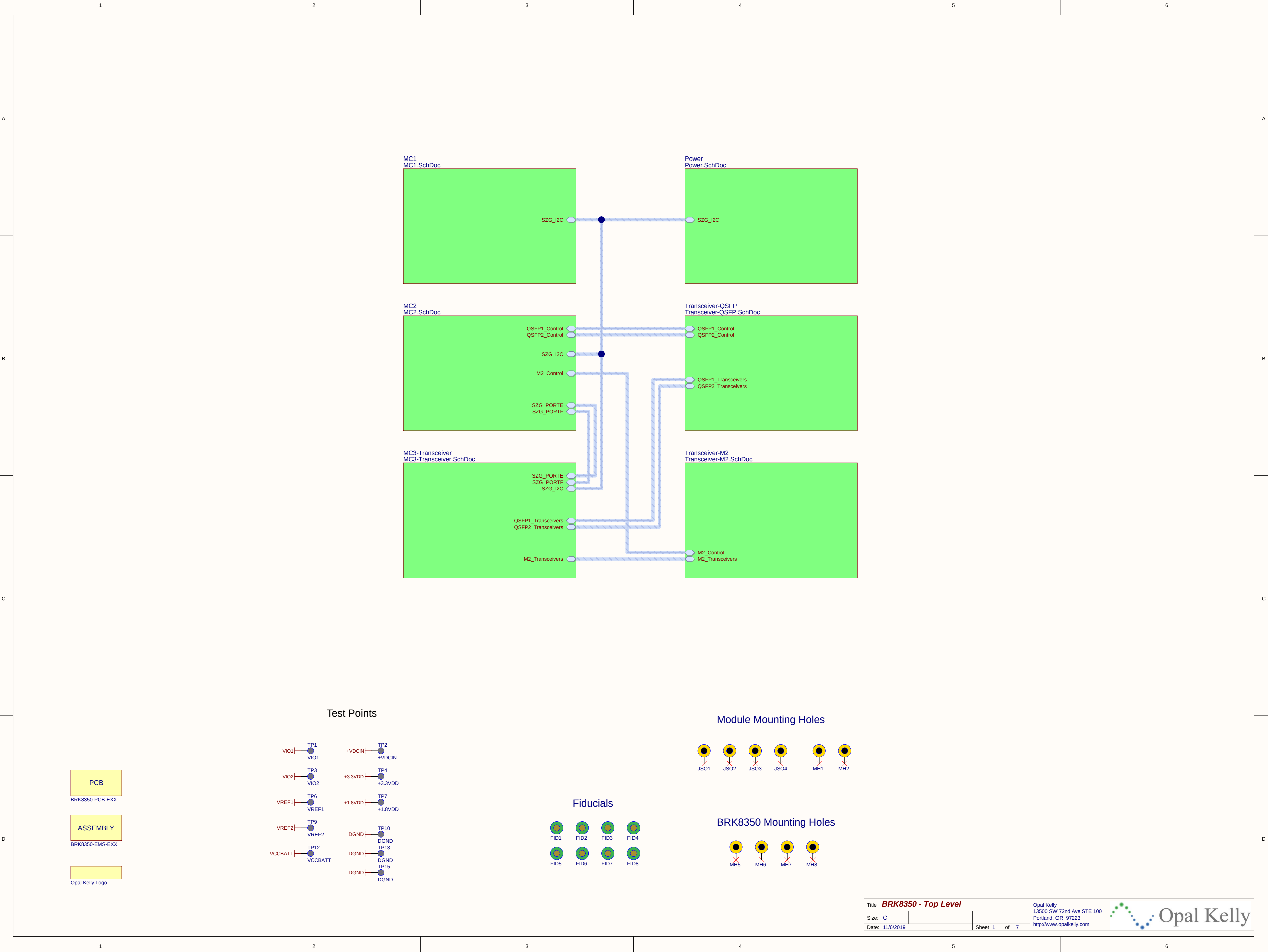
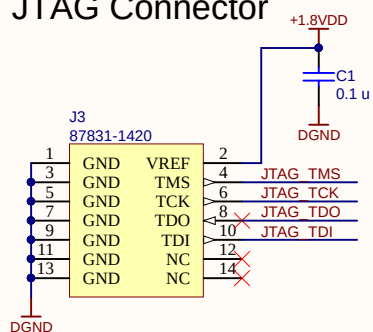


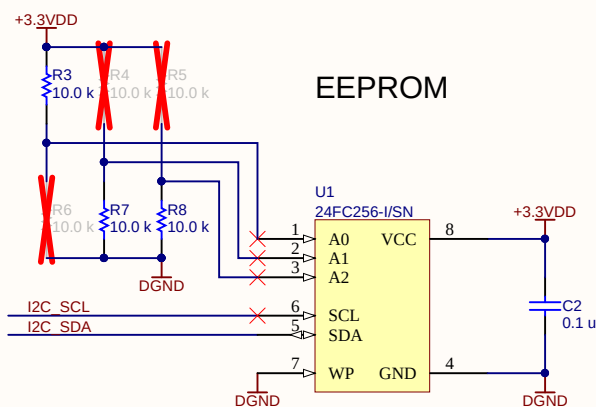


Mezzanine Connector MC1

JTAG Connector

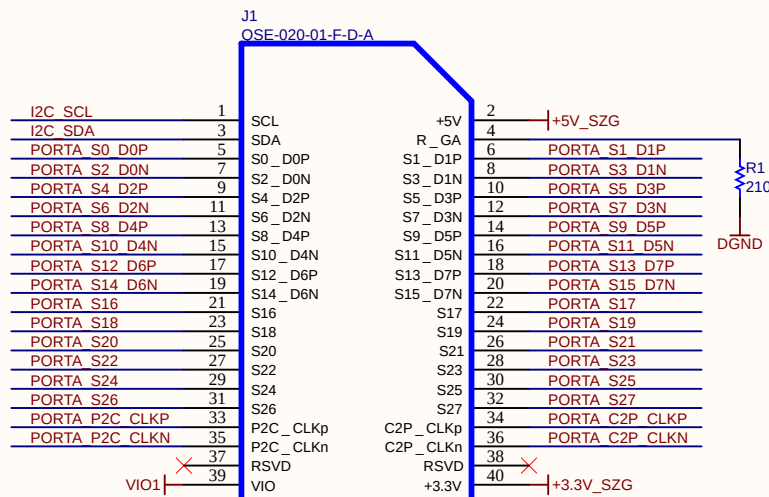


EEPROM



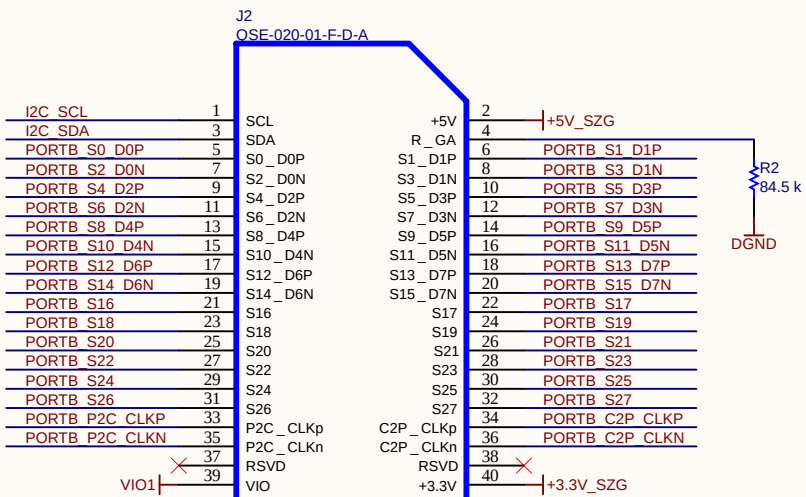
SYZYGY PORT A (VIO1)

Address 0x30

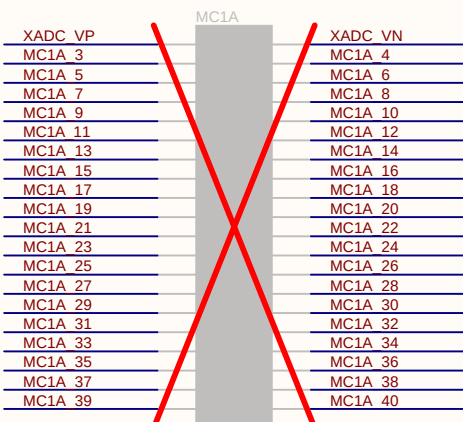
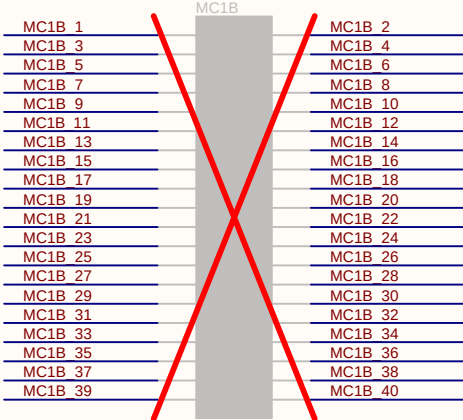
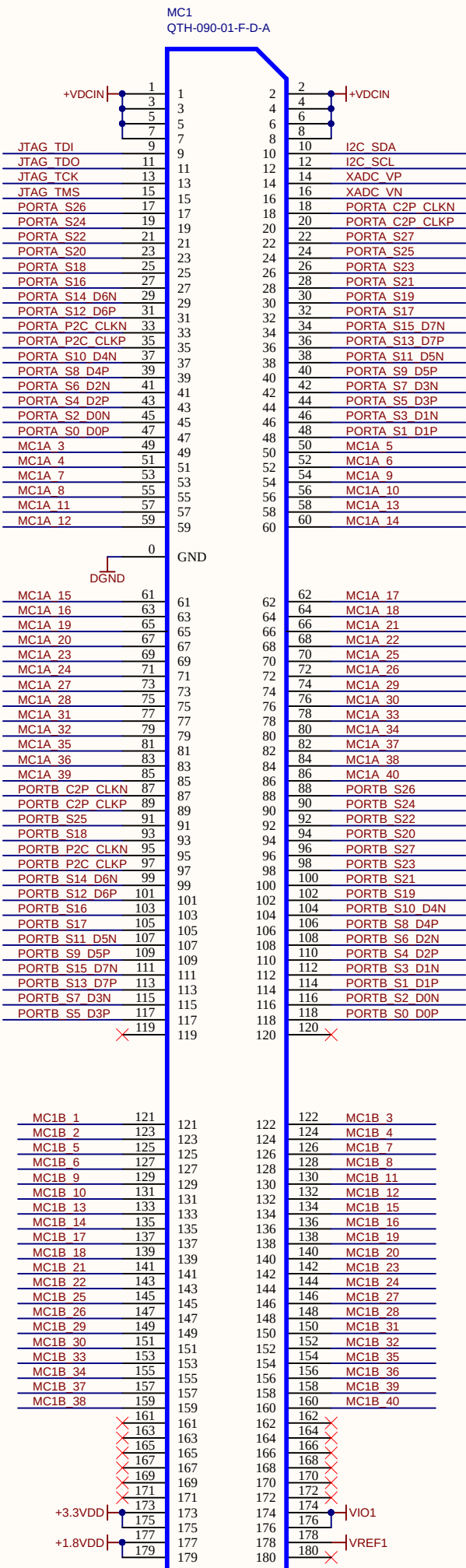


SYZYGY PORT B (VIO1)

Address 0x31



2mm Headers



MC3		OTH-060-01-L-D-DP-A	
SATA 1 TXB+	1	2	SATA 1 TXA+
SATA 1 TXB-	3	4	SATA 1 TXA-
SATA 2 TXB+	5	6	SATA 2 TXA+
SATA 2 TXB-	7	8	SATA 2 TXA-
RXP3	9	10	TXP3
RXN3	11	12	TXN3
RXP2	13	14	TXP2
RXN2	15	16	TXN2
100MHZ REFCLK P	17	18	SMA REFCLKP
100MHZ REFCLK N	19	20	SMA REFCLKN
M2 PER P3	21	22	M2 PET P3
M2 PER N3	23	24	M2 PET N3
M2 PER P2	25	26	M2 PET P2
M2 PER N2	27	28	M2 PET N2
M2 PER P1	29	30	M2 PET P1
M2 PER N1	31	32	M2 PET N1
M2 PER P0	33	34	M2 PET P0
M2 PER N0	35	36	M2 PET N0
	37	38	
	39	40	
	GND		
	41	42	
	43	44	
RXP1	45	46	TXP1
RXN1	47	48	TXN1
RXP0	49	50	TXP0
RXN0	51	52	TXN0
QSFP 2 RX1P	53	54	QSFP 2 TX4P
QSFP 2 RX1N	55	56	QSFP 2 TX4N
QSFP 2 RX2P	57	58	QSFP 2 TX3P
QSFP 2 RX2N	59	60	QSFP 2 TX3N
QSFP 2 RX3P	61	62	QSFP 2 TX2P
QSFP 2 RX3N	63	64	QSFP 2 TX2N
QSFP 2 RX4P	65	66	QSFP 2 TX1P
QSFP 2 RX4N	67	68	QSFP 2 TX1N
PORTE RX0P	69	70	PORTE TX0P
PORTE RX0N	71	72	PORTE TX0N
PORTE RX1P	73	74	PORTE TX1P
PORTE RX1N	75	76	PORTE TX1N
PORTE RX3P	77	78	PORTE TX3P
PORTE RX3N	79	80	PORTE TX3N
PORTE RX2P	81	82	PORTE TX2P
PORTE RX2N	83	84	PORTE TX2N
PORTE REFCLKP	85	86	PORTE REFCLKP
PORTE REFCLKN	87	88	PORTE REFCLKN
PORTE RX1P	89	90	PORTE TX1P
PORTE RX1N	91	92	PORTE TX1N
PORTE RX0P	93	94	PORTE TX0P
PORTE RX0N	95	96	PORTE TX0N
PORTE RX3P	97	98	PORTE TX3P
PORTE RX3N	99	100	PORTE TX3N
PORTE RX2P	101	102	PORTE TX2P
PORTE RX2N	103	104	PORTE TX2N
QSFP 1 RX1P	105	106	QSFP 1 TX4P
QSFP 1 RX1N	107	108	QSFP 1 TX4N
QSFP 1 RX2P	109	110	QSFP 1 TX3P
QSFP 1 RX2N	111	112	QSFP 1 TX3N
QSFP 1 RX3P	113	114	QSFP 1 TX2P
QSFP 1 RX3N	115	116	QSFP 1 TX2N
QSFP 1 RX4P	117	118	QSFP 1 TX1P
QSFP 1 RX4N	119	120	QSFP 1 TX1N

The diagram illustrates the QSPF1 Transceivers, which are organized into two main sections: QSPF Transceivers and QSPF1 Transceivers. The QSPF Transceivers section lists TX1P, TX1N, TX2P, TX2N, TX3P, TX3N, TX4P, and TX4N. The QSPF1 Transceivers section lists RX1P, RX1N, RX2P, RX2N, RX3P, RX3N, RX4P, and RX4N. Arrows indicate the signal flow from the QSPF Transceivers to the QSPF1 Transceivers.

QSPF Transceivers	QSPF1 Transceivers
QSPF 1 TX1P	RX1P
QSPF 1 TX1N	RX1N
QSPF 1 TX2P	RX2P
QSPF 1 TX2N	RX2N
QSPF 1 TX3P	RX3P
QSPF 1 TX3N	RX3N
QSPF 1 TX4P	RX4P
QSPF 1 TX4N	RX4N

The diagram illustrates the QSPF2 Transceivers, which are organized into two main sections: TX (Transmit) and RX (Receive). Each section contains five pairs of transceivers, labeled 1P, 2P, 3P, 4P, and 4N. The TX section is on the left, and the RX section is on the right. A central vertical line separates the two sections. A large bracket on the right side of the diagram groups all the transceivers under the label 'QSPF2 Transceivers'.

TX (Transmit)	RX (Receive)
QSPF 2 TX1P	QSPF 2 RX1P
QSPF 2 TX1N	QSPF 2 RX1N
QSPF 2 TX2P	QSPF 2 RX2P
QSPF 2 TX2N	QSPF 2 RX2N
QSPF 2 TX3P	QSPF 2 RX3P
QSPF 2 TX3N	QSPF 2 RX3N
QSPF 2 TX4P	QSPF 2 RX4P
QSPF 2 TX4N	QSPF 2 RX4N

```

graph TD
    M2_Transceivers[M2 Transceivers] --> M2_PER_N3[M2 PER N3]
    M2_Transceivers --> M2_PER_P3[M2 PER P3]
    M2_Transceivers --> M2_PET_N3[M2 PET N3]
    M2_Transceivers --> M2_PET_P3[M2 PET P3]
    M2_PER_N3 --> M2_PER_N2[M2 PER N2]
    M2_PER_N3 --> M2_PER_P2[M2 PER P2]
    M2_PER_N2 --> M2_PET_N2[M2 PET N2]
    M2_PER_N2 --> M2_PET_P2[M2 PET P2]
    M2_PER_N2 --> M2_PER_N1[M2 PER N1]
    M2_PER_N2 --> M2_PER_P1[M2 PER P1]
    M2_PER_N1 --> M2_PET_N1[M2 PET N1]
    M2_PER_N1 --> M2_PET_P1[M2 PET P1]
    M2_PER_N1 --> M2_PER_N0[M2 PER N0]
    M2_PER_N1 --> M2_PER_P0[M2 PER P0]
    M2_PER_N0 --> M2_PET_N0[M2 PET N0]
    M2_PER_N0 --> M2_PET_P0[M2 PET P0]
    M2_PER_N0 --> M2_PER_N3
    M2_PER_N0 --> M2_PER_P3
    M2_PER_N0 --> M2_PET_N3
    M2_PER_N0 --> M2_PET_P3
  
```

The four diagrams illustrate the connection of external components to the ADXL345 module. Each diagram shows a component (J15, J16, J19, J20) connected to a capacitor (C14, C15, C18, C19) and a resistor (RXP0, RXP1, RXN0, RXN1, TXP0, TXN0, TXP1, TXN1). The components are connected to DGND, RXN0, RXN1, TXN0, and TXN1.

The diagram shows two SMA connectors, J24 and J25, connected to a common ground labeled DGND. J24 is connected to the SMA_REFCLKP signal line, and J25 is connected to the SMA_REFCLKN signal line. The ground connection for both connectors is shown as a vertical line from the connector body to the DGND label.

Address 0x34

OSH-020-01-F-DP-A

J2C

J2D

Pin 1: SCL

Pin 2: +5V

Pin 3: SDA

Pin 4: +5V

Pin 5: RX0P

Pin 6: PORTE TX0P

Pin 7: RX0N

Pin 8: PORTE TX0N

Pin 9: RX1P

Pin 10: PORTE TX1P

Pin 11: RX1N

Pin 12: PORTE TX1N

Pin 13: REFCLKP

Pin 14: PORTE S0

Pin 15: REFCLKN

Pin 16: PORTE S1

Pin 17: S2

Pin 18: PORTE S3

Pin 19: S4

Pin 20: PORTE S5

Pin 21: S6

Pin 22: PORTE S7

Pin 23: S8

Pin 24: PORTE S9

Pin 25: RX3P

Pin 26: PORTE TX3P

Pin 27: RX3N

Pin 28: PORTE TX3N

Pin 29: RX2P

Pin 30: PORTE TX2P

Pin 31: RX2N

Pin 32: PORTE TX2N

Pin 33: P2C_CLKP

Pin 34: PORTE C2P_CLKP

Pin 35: P2C_CLKN

Pin 36: PORTE C2P_CLKN

Pin 37: RSVD

Pin 38: RSVD

Pin 39: VIO2

Pin 40: +3.3V

Address 0x35

Pin-to-pin connection diagram for the TXR4 module. The diagram shows two rows of pins, each with 16 pins. The left row is labeled J23 and the right row is labeled OSH-020-01E-DP-A. The TXR4 module is represented by a blue trapezoidal shape connecting the two rows. Various pins are connected, with some marked as not connected (X) or with specific components like a 4.0k resistor (R13) and a 3.3V voltage source (+3.3V_SZG).

J23 Pin	Signal	OSHA Pin	Signal	Notes
1	SCL	2	+5V_SZG	
3	SDA	4	R_GA	
5	PORTF_RX0P	6	PORTF_TX0P	
7	PORTF_RX0N	8	PORTF_TX0N	
9	PORTF_RX1P	10	PORTF_TX1P	
11	PORTF_RX1N	12	PORTF_TX1N	
13	PORTF_REFCLKP	14	PORTF_S0	
15	PORTF_REFCLKN	16	PORTF_S1	
17	PORTF_S2	18	PORTF_S3	
19	PORTF_S4	20	PORTF_S5	
21	PORTF_S6	22	PORTF_S7	
23	PORTF_S8	24	PORTF_S9	
25	PORTF_RX3P	26	PORTF_TX3P	
27	PORTF_RX3N	28	PORTF_TX3N	
29	PORTF_RX2P	30	PORTF_TX2P	
31	PORTF_RX2N	32	PORTF_TX2N	
33	PORTF_P2C_CLKP	34	PORTF_C2P_CLKP	
35	PORTF_P2C_CLKN	36	PORTF_C2P_CLKN	
37	RSVD	38	RSVD	
39	VIO2	40	+3.3V_SZG	

Additional components and connections shown in the diagram:

- 4.0k resistor (R13) connected between R_GA (pin 4) and DGND.
- 3.3V voltage source (+3.3V_SZG) connected to pin 40.
- Not connected (X) marks are present on pins 37, 39, and 40.

Diagram illustrating the mapping of external signals to internal components:

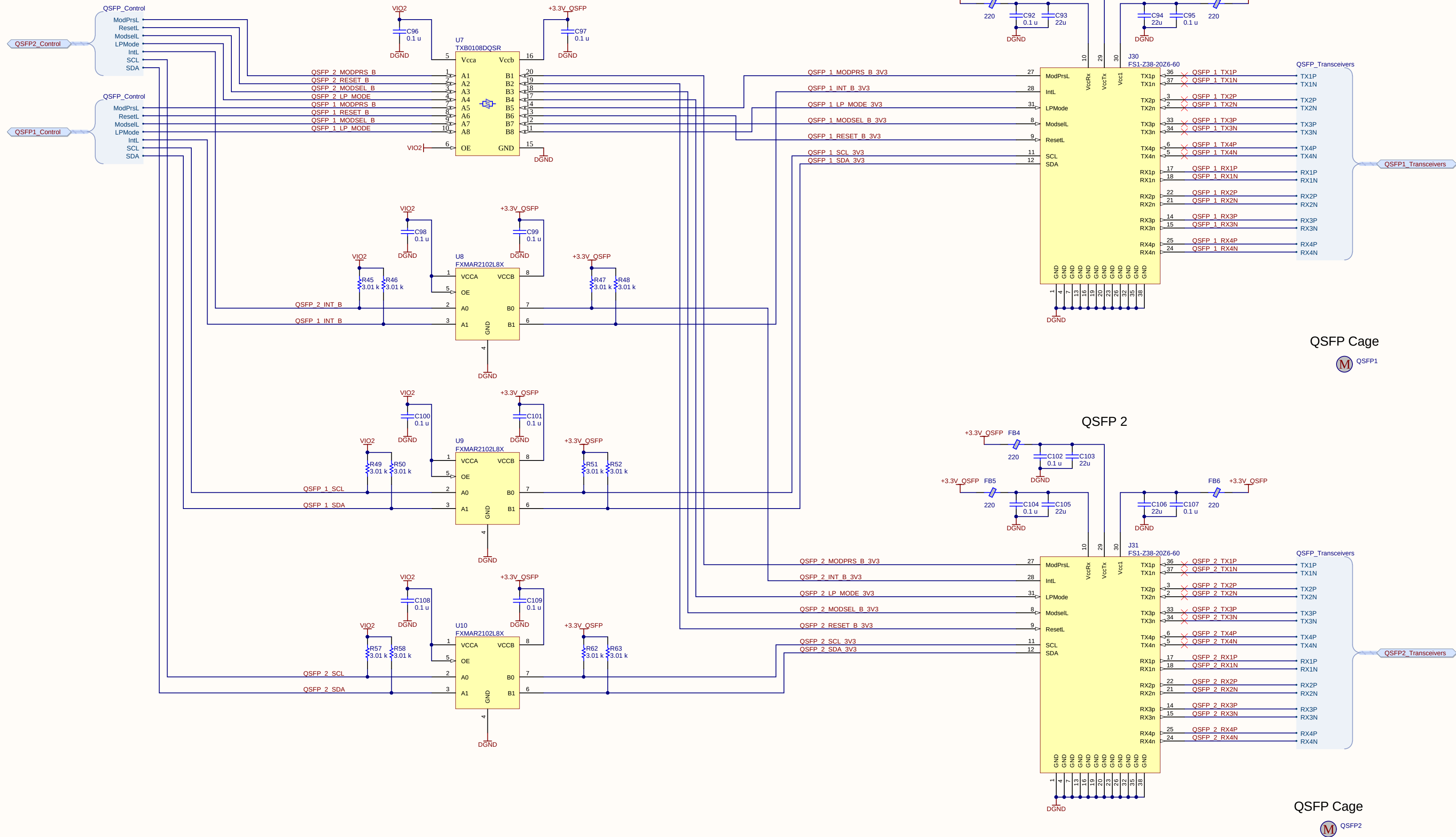
- PORT_E_S0 → PORT_S0
- PORT_E_S1 → PORT_S1
- PORT_E_S2 → PORT_S2
- PORT_E_S3 → PORT_S3
- PORT_E_S4 → PORT_S4
- PORT_E_S5 → PORT_S5
- PORT_E_S6 → PORT_S6
- PORT_E_S7 → PORT_S7
- PORT_E_S8 → PORT_S8
- PORT_E_S9 → PORT_S9
- PORT_E_C2P_CLKP → PORT_C2P_CLKP
- PORT_E_C2P_CLKN → PORT_C2P_CLKN
- PORT_E_P2C_CLKP → PORT_P2C_CLKP
- PORT_E_P2C_CLKN → PORT_P2C_CLKN

The internal components are grouped under the label **SZG_PORTE**.

Diagram illustrating the mapping of external signals to internal components:

- PORTF_S0 → PORT_S0
- PORTF_S1 → PORT_S1
- PORTF_S2 → PORT_S2
- PORTF_S3 → PORT_S3
- PORTF_S4 → PORT_S4
- PORTF_S5 → PORT_S5
- PORTF_S6 → PORT_S6
- PORTF_S7 → PORT_S7
- PORTF_S8 → PORT_S8
- PORTF_S9 → PORT_S9
- PORTF_C2P_CLKP → PORT_C2P_CLKP
- PORTF_C2P_CLKN → PORT_C2P_CLKN
- PORTF_P2C_CLKP → PORT_P2C_CLKP
- PORTF_P2C_CLKN → PORT_P2C_CLKN
- PORTF_S9 → SZG_PORTF

Level Translators



A

B

C

D

Level Translators

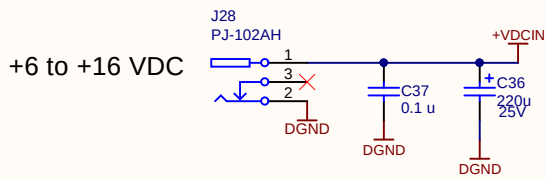
M.2 Connector

100 MHz HCSL Oscillator

M.2 Standoffs

M.2 Mounting Hardware

Power Jack



Switching Power Supply

