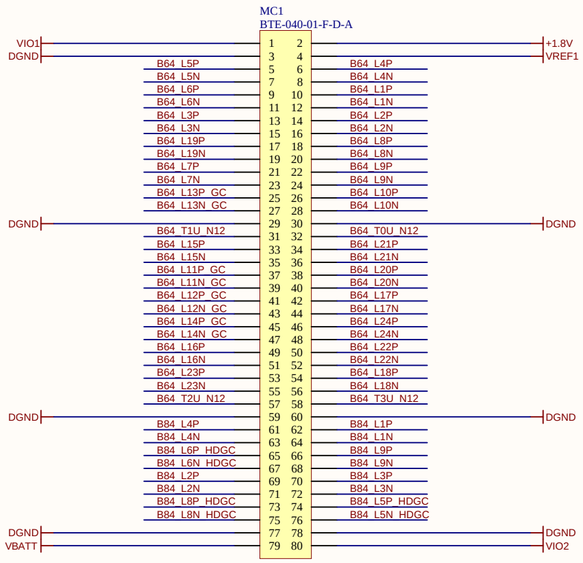
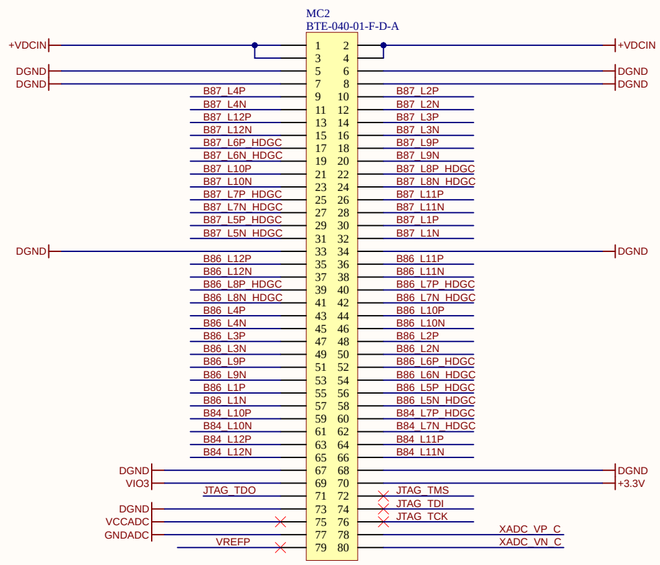
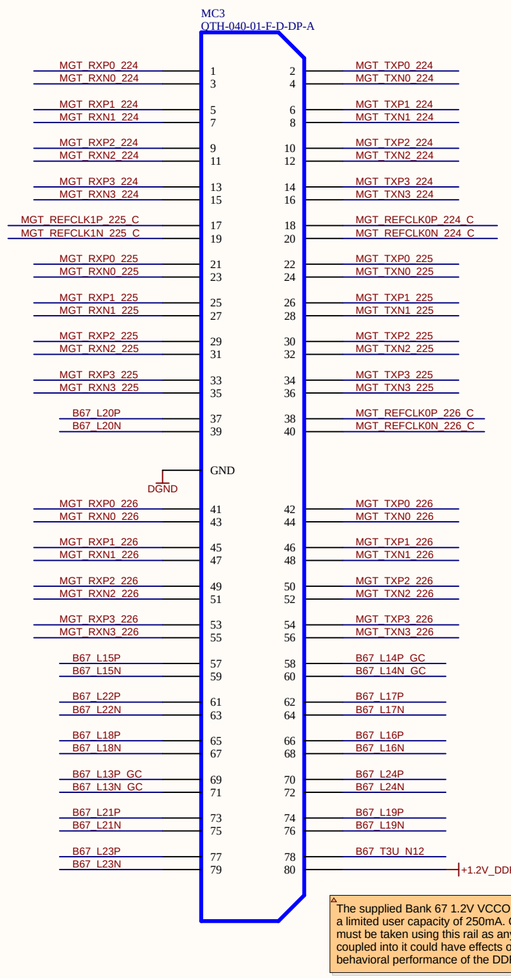
Mezzanine Connector 1



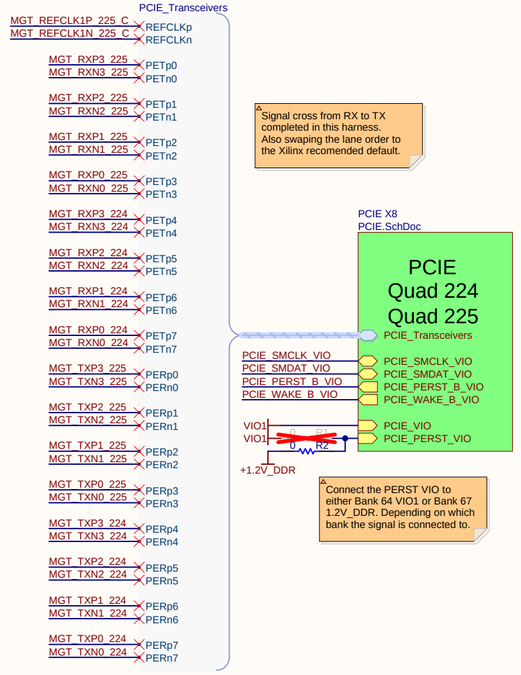
Mezzanine Connector 2



Mezzanine Connector 3



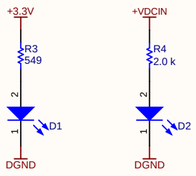
The supplied Bank 67 1.2V VCCO rail has a limited user capacity of 250mA. Care must be taken using this rail as any noise coupled into it could have effects on the behavioral performance of the DDR.



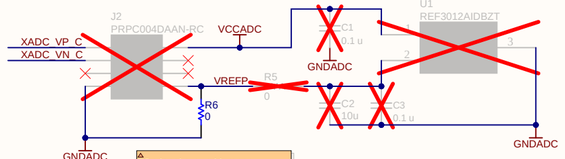
Signal cross from RX to TX completed in this harness. Also swaping the lane order to the Xilinx recomended default.

Connect the PERST VIO to either Bank 64 VIO1 or Bank 67 1.2V_DDR. Depending on which bank the signal is connected to.

Power LEDs

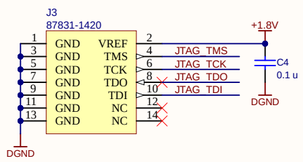


SYSMON Header

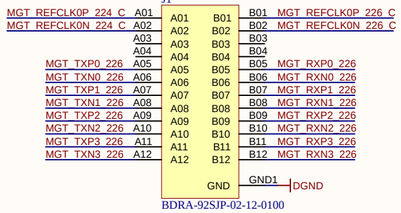


Optional ground jumper resistor to enable the internal voltage reference.

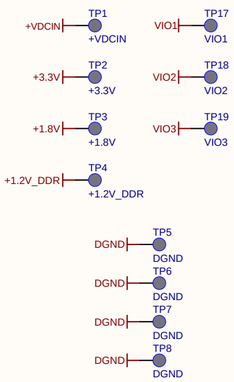
JTAG Connector

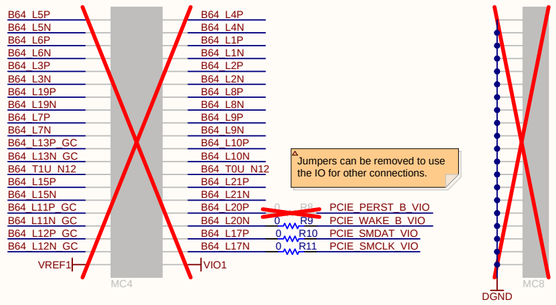


Bulls Eye

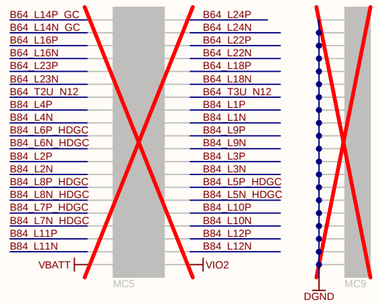


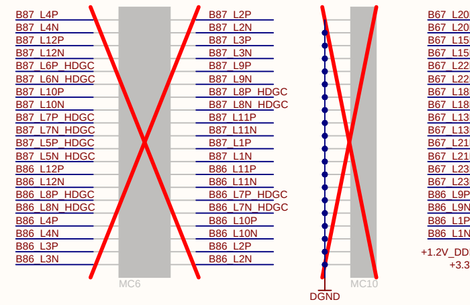
Test Points

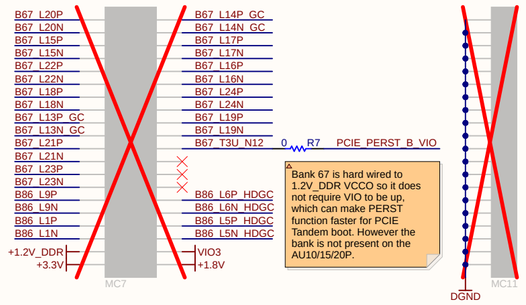




Jumpers can be removed to use the IO for other connections.







Bank 67 is hard wired to 1.2V_DDR VCCO so it does not require VIO to be up, which can make PERST function faster for PCIE Tandem boot. However the bank is not present on the AU10/15/20P.

BARCODE LABEL

LABEL-USB-SN

PCB

BRK8310-PCB-AXX

ASSEMBLY

BRK8310-EMS-AXX

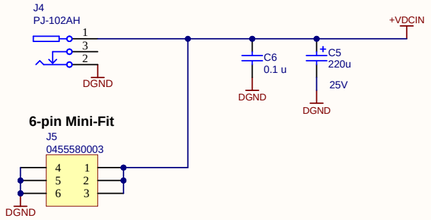
Opal Kelly Logo

Fiduciales

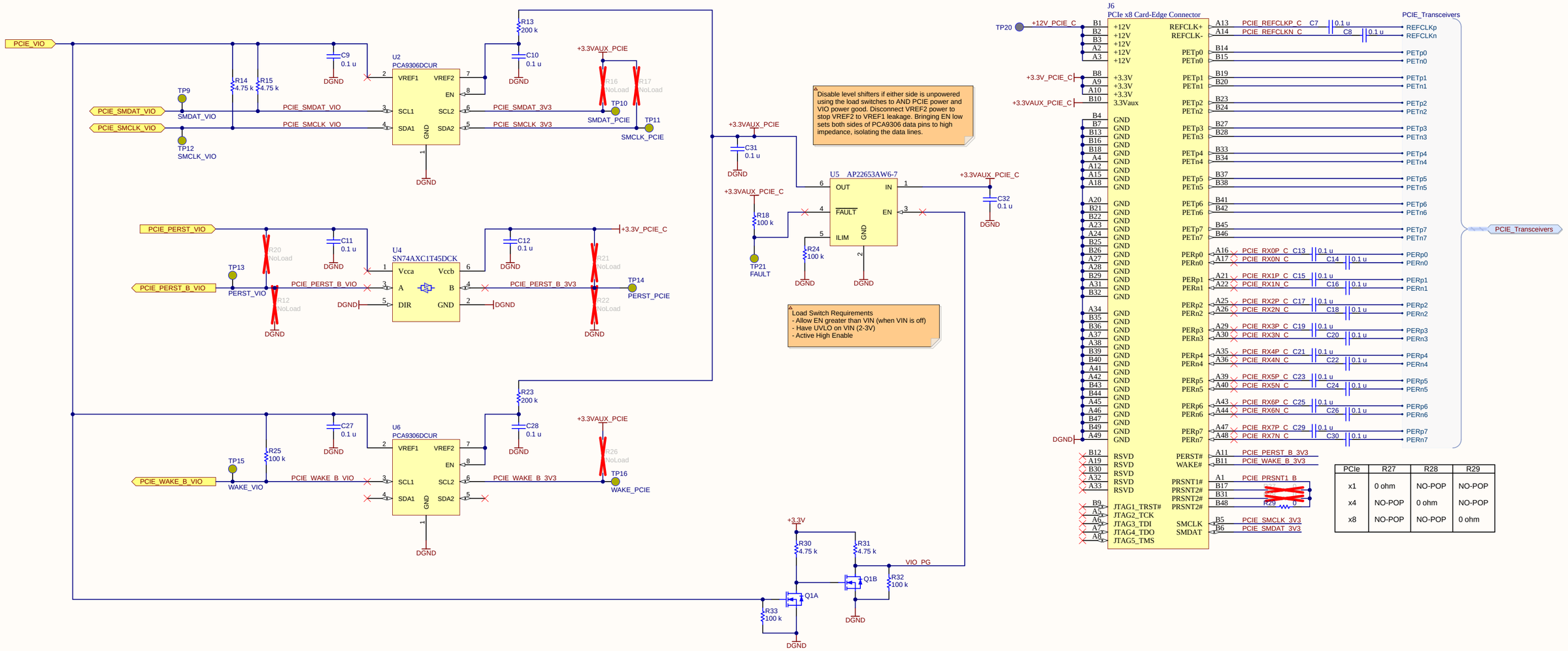
Module Mounting Holes

Power Jack

+7.5 to +15 VDC



Title: BRK8310 PCB			Opal Kelly 13500 SW 72nd Ave, STE 100 217.391.3724 http://www.opalkelly.com
Size: C	Number: 1	Revision: A 01	
Date: 5/19/2022 Time: 1:11:12 PM		Sheet 1 of 2	
Drawn by: RCA			



PCIe x8 Edge Connector

PCIe	R27	R28	R29
x1	0 ohm	NO-POP	NO-POP
x4	NO-POP	0 ohm	NO-POP
x8	NO-POP	NO-POP	0 ohm

Title: BRK8310 - PCIE			Opal Kelly 13500 SW 72nd Ave, STE 100 217.391.3724 http://www.opalkelly.com
Size: C	Number: 2	Revision: A 01	
Date: 5/19/2022	Time: 1:11:12 PM	Sheet 2 of 2	
Drawn by: RCA			